A Novel Flip Chip Bonding Technology using Au Stud Bump and Lead-free Solder

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ABSTRACT
A cost-effective Au-solder flip-chip bonding technology working with unique designs of bonding pads and solder resist on organic substrate has been developed. The increasing demand for smaller and lighter system module, and the design requirements for electrical and thermal enhancement drive the deployment of flip chip technologies. Existing flip chip technologies are briefly reviewed and compared; the key design techniques and solder selection to drive the process improvement are explained in details the process improvements include: 1. Excellent void control over underfill resin; 2. Formation of uniform solder humps on the bonding pads of the substrate; 3. Selection of non-lead solder to enhance interconnection reliability. A 5-chip MCM design example is shown for the improvement of bonding time; a test vehicle used for reliability tests is described, the result of reliability tests confirms Au-solder flip chip bonding technique is a sound bonding process.

Key words: Flip Chip, Au-solder, Super Juffit®, Build-up

INTRODUCTION
As the handheld device usage keeps on expanding in consumer market, the demand for smaller, thinner and lighter system modules are projected to be increasing rapidly. The stud bump technologies [1] [2] [3], widely used as direct chip attachment on miniaturized system boards, will continue providing flip chip bonding option for the device designed for wirebonding.

Compared to area-array bumping technology, like C4 or eutectic solder bump, stud bump has the clear advantages as follows:
- Capable of handling much finer pad pitch, 100um or below;
- Require no signal re-distribution layer;
- Bump formation process is simple and straightforward;
- Low equipment cost.

The purpose of this study is to investigate a cost effective flip chip technology, which will achieve 1) Throughput improvement of flip chip bonding process; 2) Void-free underfill process; 3) Lower assembly cost.

REVIEW OF FLIP CHIP TECHNOLOGY
There are at least five existing flip chip technologies currently being used. Shown in Figure 1, they are briefly reviewed as follows:

Solder Bump Bonding
Wafer bumping and adding signal re-distribution layer for the devices with peripheral-pad design are required before flip-chip bonding starts. Solder-bumped chip is bonded on an Au plated or solder pre-coated pads on the substrate. Strong and reliable connection will be formed along with underfill resin. Under barrier metal and solder bump process are needed and conventional Al padded chip can not be used.

Au Bump on Au Plated Substrate
Au stud bump formed on a chip is bonded to plated Au pads on the substrate with high temperature and high bonding pressure. The connection is made via Au-to-Au metal bonding. This technique can only be used on ceramic substrate due to high-temperature and -pressure process involved.

Au Bump with Conductive Paste
After forming stud bumps on die and before flip bonding starts, small amount of conductive paste is transferred to the tip of the Au stud bumps, non-conductive epoxy is dispensed on the center part of die bonding area, then chip is pressed against the substrate after the bonding alignment. Mild pressure and heat are applied at the backside of the die, both the underfill resin and conductive paste are cured simultaneously. The bonding time takes larger than 30 seconds, which is longer than other techniques. It is compatible with organic substrate.

Au Bump with Anisotropic Conductive Adhesive
Compared to the technique mentioned above, it uses anisotropic conductive paste instead of conventional conductive paste and can handle the finer pitch bonding potentially. However, it has the same drawback as Au / Conductive Epoxy – lower throughput due to the long bonding time.

Au Bump with Solder
Au stud bumps on the chip are bonded to the substrate through pre-coated solder on bonding pads. This technique achieves the shortest bonding time and improves the manufacturing throughput dramatically. However, the challenge is how to coat a thin uniform solder layer on the pads.
Figure 1: Flip Chip Bonding Technologies

Selection Criteria for a Flip Chip Bonding Technology
The following criteria are used to select Au-solder flip chip bonding technology over the others listed above:

- Short machine time, in other words, low machine cost;
- Compatible to organic substrate;
- Conventional Al padded chip can be used.

Au-SOLDER FLIP CHIP TECHNOLOGY Structure
Cross sectional diagram and photo of Au-solder bonded chip are shown in Figures 2(a) and (b) respectively. Au stud bumps formed on the chip are bonded to solder pre-coated pads on the substrate to make electrical and mechanical connection. Underfill resin is applied to the edge of die and fills the gap between active chip surface and the substrate. The resin enhances Au-solder bonding and offers highly reliable interconnection.

Figure 2a: Cross Sectional Structure of Au-solder Bonded Chip

Au-bump Formation
Au stud bump is formed by "stud bonding machine", similar to conventional Au ball bonding machine. Stud bump is made of Au bonding wire through following processes:

- Form gold ball at the end of the Au wire by electric discharge;
- Bond the Au ball on the Al pad with ultrasonic energy and bonding force;
- Cut the Au-wire by pulling it;
- Apply force again the stud bumps with the flat surface of a leveling block and make the top of the Au studs even.

To have good control over the variation of bump height before applying the leveling process, the Au wire that has higher Vickers Hardness was used, the variation is within +/- 5µm. See Table 1 for Vickers Hardness specification of both gold wires for stud bump and wirebonding bonding.

Table 1: Vickers Hardness of Au Wire

<table>
<thead>
<tr>
<th>Usage</th>
<th>Vickers Hardness</th>
</tr>
</thead>
<tbody>
<tr>
<td>Stud bump</td>
<td>About 95 Hv</td>
</tr>
<tr>
<td>Wirebonding</td>
<td>About 75 Hv</td>
</tr>
</tbody>
</table>

Solder Pre-coating
Lead-free solder, instead of eutectic one, was chosen to bond Au-bumped die to the substrate. Based on bump resistance variation during high-temperature life test, shown in Figure 3, the interconnection using stud bumps / eutectic solder started to deteriorate after 300-hour exposure, however, there is no significant resistance change observed for the connections made by lead-free solder. Cross sectional analysis for the root cause of failed connection using eutectic solder did find that eutectic solder had settled into two phases, Lead (Pb)-rich phase and Tin (Sn)-rich one. This phase separation effect weakens the solder strength and, thus causes electrical connection failure.
To achieve a flat and uniform solder coating on bonding pads, Super Juffit® (SJ) technique, developed by Showa Denko K.K., was selected for solder pre-coating on an organic substrate. SJ process steps, shown in Figure 4, is briefly described as follows:

- Organic substrate, with bare Cu trace, is treated with weak acid to remove thin Cu oxide layer. To use this technique, clean Cu surface, with no flux and oxidation inhibitor, is required.
- Treat the substrate with special chemical that makes Cu surface sticky.
- Apply solder powder to the sticky layer on the Cu trace and form thin powder layer. By controlling the powder diameter, the final solder thickness can be well controlled by carefully selecting the size of solder powder.
- Apply soldering flux and melt solder powder.
- Solder humps are formed
- Clean flux residue.

The advantages of using this technique include 1) High productivity; 2) Capable of handling fine-line coating and 3) Simple and low-cost process.

### 2.4 Underfill Resin

The application of underfill resin will mechanically reinforce Au-solder bonding and it is the key material / process to make highly reliable flip chip interconnection. Acid Anhydride Epoxy with silica filler was used. See Table 2 for its major material properties. Acid anhydride epoxy has strong adhesion force and low moisture absorption rate. Since the resin has rather high viscosity, 12000 cps, to ensure smooth resin flow within the gap between the chip and the substrate, the diameter of silica filler and its volume content are carefully determined and controlled. The gap with the minimum height, 40 μm, can be filled with the selected underfill resin without the hassle. In addition, with high glass transition temperature, 140 degree C and low C.T.E., 26 ppm/degree C, this resin is a good choice used for high reliability interconnection.

<table>
<thead>
<tr>
<th>Resin</th>
<th>Acid anhydride epoxy</th>
</tr>
</thead>
<tbody>
<tr>
<td>Viscosity</td>
<td>12000 cps</td>
</tr>
<tr>
<td>Tg</td>
<td>140 degree C</td>
</tr>
<tr>
<td>C.T.E.</td>
<td>26 ppm/degree C</td>
</tr>
</tbody>
</table>

Table 2: Physical Properties of Underfill Resin

### Solder Resist Design

The design of solder resist pattern is another key process in the development of Au-solder flip chip technology. The design goal is to make the flow of underfill resin within the gap between the chip and the substrate is free of voids, which may induce the metal corrosion of the chip.

To have better understanding of the resin flow under the capillary force, we conducted the experiments using a transparent test chip, made of glass. Two types of solder resist patterns, called N and W, were used. Refer to Figure 5 for the flow of underfill resin. Type N has narrower opening at the area designated as N (o), where the chip and the solder resist pattern are overlapped, for type W substrate, it has wider openings at W (o), which has no overlapped area near the edge of the chip.

We applied the underfill resin at the one side of the chip and observed the resin flow through glass chip. For N type of substrate, the resin flows faster in zones N(i) and N(o) when the flow hits the solder resist at the far-end corner of the chip, the resin in zones N(i) and N(o) merges and makes a void. In contrast, for W type one, the resin flows at zone W(m) and W(o) are always slower than that at W(i), and there is no void observed through underfilling process. As the result of this experiment, W solder resist pattern becomes the preferable design in our process.
**Bond Pad Design**

Another advantage of using Type W solder resist design is the longer bare copper traces with the design tends to have the smaller variation of the thickness the pre-coated solder. The reason is the larger amount of solder particles required for each copper trace can produce the smaller variation of solder volume in terms of probability when the size of solder particles is in the wide range. Therefore, Type W solder resist gives us the better control of solder thickness.

The drawback of this design is it may form a solder hump in a random location along the copper trace. In Figure 6, it shows several pre-coated solder shapes for the bonding pad design with various pad widths. When the pad width is reduced to 60 um, there is a solder hump formed along the trace. Per the experiment, we found the location of the hump can be varied trace by trace, which has long and narrow shape. With the unpredictability of the occurrence of solder hump, this design / process can not be used for solder pre-coating.

To have good control over the location of solder hump on each copper trace, we came out a novel bonding pad design, shown in Figure 7. In this design, the wider trace is used for the designated bond pad area, so that the solder hump will be always formed at that location. In addition to the hump location, solder volume should be well controlled so that the height of the solder hump is adequate for the Au stud bonding. Actual pad design depends on many parameters such as the diameter of the solder powder, pad width and pad length, which can be determined by experiment.

An example of the top-layer substrate design is shown in Figure 8. Doted line represents the outline of LSI chip; the area surrounding by two solid-line squares is a solder resist opening. For any copper trace, the bond pad area uses the wider trace.

**Au-solder Flip Chip Bonding Process**

Au-solder bonding process flow is depicted in Figure 9. Au
stud bumps are formed on a LSI chip with stud bonding machine, the tips of Au bumps are leveled against the flat surface of a leveling block, then the bumped die is set for flip chip bonding process. After optically aligned with the substrate, it is pressed against the bonding pad and heated to melt the pre-coated solder to make the connection. To enhance the interconnect reliability, underfill resin is applied along one side of die, and fill the gap between chip and substrate under capillary force, the final process step is to put the whole package into an oven for cure.

An MCM Design Example
An MCM design example is shown in Figure 10. Four LSI and one SSI die are mounted on a 19 x 19 mm² organic substrate using Au-solder bonding technique. For the flip chip bonding process, it takes less than 1 minute to complete chip mounting on a 5-chip MCM, the throughput of flip-chip bonding is about 10 seconds per chip.

RELIABILITY TEST
Description of A Test Vehicle
A test vehicle was developed to confirm the design and processes used in Au-solder bonding technique. The substrate consists of FR-4 core and 2 build-up layers on both top and bottom sides of it. Substrate size is 19mmx19mmx1mm. Test chip measures at 7.45mmx5.34mmx0.6mm.

Reliability Test and The Results
Reliability tests and the results are summarized in Table 3. Liquid-to-liquid thermal shock test was chosen to replace temperature cycling one since it provides more severe test condition to the bump interconnection. The samples, subjected to pre-conditioning test, passed 1000 cycles with temperature range between –55 °C to +125 °C.

High temperature storage test was used to check the metallurgical stability of the bonding structure. We confirmed the diffusion of Au to lead-free solder has no significant impact to the reliability of interconnection.

Also, under high temperature and high humidity environment, the adhesion of the underfill resin to the substrate and chip and the stability of insulation resistance of the resin were confirmed. The resistance variations of the daisy chain throughout each reliability test are shown in Figures 12, 13 and 14 respectively. The criterion to judge the bump interconnect reliability is the resistance increase shall be less than 20 mohm per bump connection, or 0.44 ohm per a daisy chain.
### Table 3: Reliability Tests and the Results

<table>
<thead>
<tr>
<th>Test Item</th>
<th>Conditions</th>
<th>Sample Size</th>
<th>Test Results</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thermal Shock</td>
<td>-55 °C, 5 min. ↔125°C, 5 min.</td>
<td>10 chains</td>
<td>1000 cycles Passed</td>
</tr>
<tr>
<td>High Temperature Storage</td>
<td>125 °C</td>
<td>8 chains</td>
<td>1500 hours Passed</td>
</tr>
<tr>
<td>High Temperature Humidity with Bias</td>
<td>85 °C, 85% RH 5V</td>
<td>10 chains</td>
<td>1500 hours Passed</td>
</tr>
</tbody>
</table>

(Note: All samples are subjected to preconditioning test with the following test conditions: 1) Bake at 125 degree C for 24 hours; 2) Soak at 30 degree C and 80%RH atmosphere for 72 hours; 3) IR reflow at 235 degree °C (10 seconds) for 3 times.)

### CONCLUSION

An Au-solder flip chip technology used with organic substrate was developed. Using a novel solder resist design on substrate along with Super Juffit® solder coating technique, the reliable bump interconnection with void-free resin underfilling can be made cost-effectively. The flip chip bonding time has been reduced significantly to improve the throughput.

Au-solder flip chip technology, developed for the miniaturized MCM originally, can be expanded into single-chip packaging, especially for those devices used in RF applications. The minimum pad pitch used in existing designs, 100 um, targets to be reduced to less than 85 um.

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### REFERENCES


